

Fig. 2

No. 100 No.	Analog Test Matrix	st Matrix																
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Test Stead	Pln_Name			ASIPOS		TEST	TEST2			_	OSC2	8				8	NIN	QQ.
The filter control of the control	Pin_Name_Analog																	
The Street Stand Section Secti	Pin_Name_Digital																	
TradeRead Mark Processed Processed	Pin_Name_Test_Mode																	
The strain The parameter	Signal_Type_Digital			8		8	_	-	_					o	۵			
The strains Section	Signal Type Analog			۵	9	_					0				Δ	g		
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1	Method A 6.2-1 Method B 6.2-2			00//00	1	0V / @01 0		1 1	.1 1	00/0001	0V / @01 0V / @03	3/ / @0-0	VO 000 V	/ @0 GNC		OND		V/@01 V/@03
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Main			ļ	200	QN 5	100	X.	PGI	- E	Poly		FG2 EK	52 E		-			40
Main	Transmitter Test			100														
	Method 8SP01 6.15	Istep(15)	#01 #08	300	GND	PG1	G1 & PG	PG1	PGT	PG:		P62.	62 P.	Z CNE				ş
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VII.=0V Sequencen (201 force value -100uA to be transferred to know-how-library VIII.=5V Sequencen (201 1) 1) Clemp=5.4V Sequencen (201 1) Clemp (201 1	Voltage Relationship (Uout / L	П	#04 AW1	AWO1		AWI1						\parallel						
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Clamp=5.4V Sequencen (@0.2 force value -1.00.uA 1.00.uA	1	A 4.			Caamp	۸۶-	Š.	tneuceu (@n1	2 2		ection	T	-	-				
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	Ana	Analog Test Matrix	Matrix	PIN1	PIN2	PIN3	PIN4	SNIA	PIN6	PiN7	PIN8	PIN9			
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Sequencer	Spec	fime sequence													
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	!		COGGINIII									-			
			measure												
			low limit		_			4.75V							
			high limit					5.25V							
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	1.3	2	LoadMax1												
			measure												
			low limit					4.75V							
			high limit					5.25V							
	1.4	3	LoadMax2										-		
			measure												
			low limit					4.75V							
			high limit					5.25V							
	2.0		. WakeUp Circuit	and the state of t	Mega, a			The first of the second							
					4.5V										
	2.1		Setupname	10V		1uF	50	5.25V		I	open	I			
	2.2	1	TestMode			Run	pattern for	Run pattern for analog Test mode	ode				<u>و</u>	Commandbuttonil	
	2.3	2	IDDsleep				`	* <20uA		pulse 1us					
	<u></u> ;					5.3V									
	4.4	2	Supeor												
	2.5	4	Sup5Off				4.5V			1	8V * <1uA				

Fig. 4

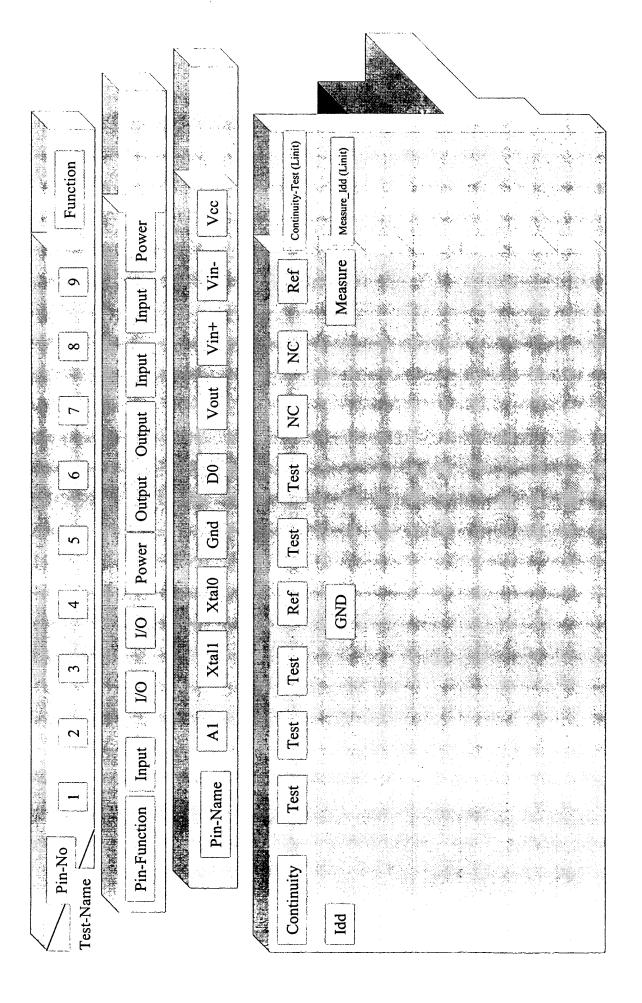


Fig. 5

